

Benjamin C. Lee

Curriculum Vitae

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benjamin.c.lee@duke.edu
Nationality: United States
Place of Birth: California

Pratt School of Engineering
Duke University
210 Hudson Hall, Box 90291
Durham, NC 27708

Interests

Energy-efficient architectures – adaptive, heterogeneous, accelerated processors.
High-performance applications – numerical, scientific, parallel computing.
Scalable technologies – emerging technologies, efficient circuits, process variations.
Design methodologies – statistics, machine learning for computer systems.
Technology policy – technology, economics, policy for environmentally sustainable IT.

Education

Harvard University

Ph.D., Computer Science, 2008.
S.M., Computer Science, 2006.
Minor, Statistics.

University of California, Berkeley

B.S., Electrical Engineering and Computer Science, 2004.
Minor, Business Administration.

Experience

Duke University, Durham NC

Assistant Professor, Electrical and Computer Engineering, 2010 – present
Assistant Professor, Computer Science, 2010 – present

Stanford University, Stanford CA

NSF Computing Innovation Fellow, Electrical Engineering, 2009 – 2010

Microsoft Research, Redmond WA

Post-doctoral Researcher, Systems and Networking, 2008 – 2009

Harvard University, Cambridge MA

Graduate Researcher, Engineering and Applied Sciences, 2004 – 2008

Intel Corporation, Santa Clara CA

Intern Researcher, Microarchitecture Research, 2007

Lawrence Livermore National Laboratory, Livermore CA

Intern Researcher, Applied Scientific Computing, 2006

University of California, Berkeley CA

Undergraduate Researcher, Computer Science, 2002 – 2004

Charles M. Salter Associates, San Francisco CA

Intern Engineer, Transportation and Airport Acoustics, 2000

Honors

2011 CAREER Award, National Science Foundation

2011 Google Faculty Research Award

2011 Research Highlight, Communications of the ACM

- “Understanding sources of inefficiency in general-purpose chips.”
- With Hameed, Qadeer, Wachs, Azizi, Solomatnikov, Richardson, Kozyrakis, and Horowitz.

2010 Research Highlight, Communications of the ACM

- “Phase change memory and the quest for scalability.”
- With Ipek, Mutlu, and Burger.

2010 Top Picks from Computer Architecture Conferences, IEEE Micro Magazine

- “Phase change technology and the future of main memory.”
- With Zhou, Yang, Zhao, Ipek, Mutlu, and Burger.

2009 Computing Innovation Fellowship, National Science Foundation

- “Rethinking digital design.”
- With Horowitz.

2008 Best Paper Nomination, IEEE Int’l Symp. Microarchitecture (MICRO)

- “CPR: Composable performance regression for scalable multiprocessor models.”
- With Collins, Wang, and Brooks.

2008 Harvard University Nomination, ACM Doctoral Dissertation Award

- “Statistical inference for efficient microarchitectural analysis.”

2008 Invited Participant, 38th St. Gallen Symposium

- “Corporate social responsibility and the globalization of ‘local values’.”

2007 Invited Participant, 37th St. Gallen Symposium

- “Flattening the world efficiently: Digital sustainability for the twenty-first century.”

2006 First Place, Student Research Competition, IEEE/ACM Supercomputing (SC)

- “Statistical inference for efficient microarchitectural and application analysis.”

2004 Engineering and Applied Sciences Fellowship, Harvard University

2004 Best Paper, Int’l Conf. Parallel Processing (ICPP)

- “Perf. models for evaluation & auto. tuning of symm. sparse matrix-vector multiply.”
- With Vuduc, Demmel, and Yelick.

2002 Best Student Paper Finalist, IEEE/ACM Supercomputing (SC)

- “Performance optimizations and bounds for sparse matrix-vector multiply.”
- With Vuduc, Demmel, Yelick, Kamil, and Nishtala.

2000 National Merit Scholarship

Publications

Books, Journals, Magazines

1. Rehan Hameed, Wajahat Qadeer, Megan Wachs, Omid Azizi, Alex Solomatnikov, Benjamin C. Lee, Stephen Richardson, Christos Kozyrakis, Mark Horowitz. “Understanding sources of inefficiency in general-purpose chips,” *Communications of the ACM (CACM), Research Highlight*, 54(10):85-93, October 2011.
2. Vijay Janapa Reddi, Benjamin C. Lee, Trishul Chilimbi, Kushagra Vaid. “Mobile processors for energy-efficient web search,” *ACM Transactions on Computer Systems (TOCS)*, 29(4):9.1-9.39, August 2011.
3. Ofer Shacham, Omid Azizi, Megan Wachs, Wajahat Qadeer, Zain Asgar, Kyle Kelley, Pete Stevenson, Alex Solomatnikov, Amin Firoozshahian, Benjamin C. Lee, Stephen Richard-

- son, Mark Horowitz. “Why design must change: Rethinking digital design,” *IEEE Micro Magazine*, 30(6):9-24, November/December, 2010.
4. Benjamin C. Lee, David Brooks. “Applied inference: Case studies in microarchitectural design,” *ACM Transactions on Architecture and Code Optimization (TACO)*, 7(2):1-37, October 2010.
 5. Benjamin C. Lee, Engin Ipek, Onur Mutlu, Doug Burger. “Phase change memory architecture and the quest for scalability,” *Communications of the ACM (CACM), Research Highlight*, 53(7):99-106, July 2010.
 6. Benjamin C. Lee, Ping Zhou, Engin Ipek, Onur Mutlu, Jun Yang, Youtao Zhang, Bo Zhao, Doug Burger. “Phase change technology and the future of main memory,” *IEEE Micro Magazine, Top Picks from the Computer Architecture Conferences*, 30(1):131-141, January/February, 2010.
 7. Benjamin C. Lee and D. Brooks. “A tutorial in spatial sampling and regression strategies for microarchitectural analysis,” *IEEE Micro Magazine, Special Issue on Hot Tutorials*, 27(3):74-93, May/June 2007.

Refereed Conference Proceedings

8. Omid Azizi, Aqeel Mahesri, Benjamin C. Lee, Sanjay J. Patel, Mark Horowitz. “Energy performance tradeoffs in processor architecture and circuit design: A marginal cost analysis,” in *Proc. 37th ACM International Symposium on Computer Architecture (ISCA)*, June 2010.
9. Rehan Hameed, Wajahat Qadeer, Megan Wachs, Omid Azizi, Alex Solomatnikov, Benjamin C. Lee, Stephen Richardson, Christos Kozyrakis, Mark Horowitz. “Understanding sources of inefficiency in general-purpose chips,” in *Proc. 37th ACM International Symposium on Computer Architecture (ISCA)*, June 2010.
10. Vijay Janapa Reddi, Benjamin C. Lee, Trishul Chilimbi, Kushagra Vaid. “Web search using mobile cores: Quantifying and mitigating the price of efficiency,” *Proc. 37th ACM International Symposium on Computer Architecture (ISCA)*, June 2010.¹
11. Jeremy Condit, Edmund B. Nightingale, Christopher Frost, Engin Ipek, Benjamin Lee, Doug Burger, Derrick Coetzee. “Better I/O through byte-addressable, persistent memory,” *Proc. 22nd ACM Symposium on Operating Systems Principles (SOSP)*, October 2009.
12. Xiaoyao Liang, Benjamin C. Lee, Gu-Yeon Wei, David Brooks. “Design and test strategies for microarchitectural post-fabrication tuning,” *Proc. 27th IEEE International Conference on Computer Design (ICCD)*, October 2009.²
13. Kristen Lovin, Benjamin C. Lee, Xiaoyao Liang, David Brooks, Gu-Yeon Wei. “Empirical performance models for 3T1D memories,” *Proc. 27th IEEE International Conference on Computer Design (ICCD)*, October 2009.³
14. Benjamin C. Lee, Engin Ipek, Onur Mutlu, Doug Burger. “Architecting phase change memory as a scalable DRAM alternative,” *Proc. 36th ACM International Symposium on Com-*

¹ Also Microsoft Technical Report MSR-TR-2009-105, August 2009.

² Also Harvard University Computer Science Technical Report TR-06-08, December 2008.

³ Also Harvard University Computer Science Technical Report TR-03-08, October 2008.

puter Architecture (ISCA), June 2009.⁴

15. Benjamin C. Lee, Jamison Collins, Hong Wang, David Brooks. “CPR: Composable performance regression for scalable multiprocessor models,” *Proc. 41st IEEE International Symposium on Microarchitecture (MICRO)*, November 2008.⁵
16. Benjamin C. Lee. “Corporate social responsibility and the globalization of ‘local values,’” *38th St. Gallen Symposium: Global Capitalism – Local Values*, May 2008.
17. Benjamin C. Lee, David Brooks. “Efficiency trends and limits from comprehensive microarchitectural adaptivity,” *Proc. 13th ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, March 2008.
18. Benjamin C. Lee, David Brooks. “Roughness of microarchitectural design topologies and its implications for optimization,” *Proc. 14th IEEE International Symposium on High Performance Computer Architecture (HPCA)*, February 2008.
19. Benjamin C. Lee. “Flattening the world efficiently: Digital sustainability for the twenty-first century,” *37th St. Gallen Symposium: The Power of Natural Resources*, May 2007.
20. Benjamin C. Lee, David Brooks, Bronis de Supinski, Martin Schulz, Karan Singh, Sally McKee. “Methods of inference and learning for performance modeling of parallel applications,” *Proc. 12th ACM Symposium on Principles and Practice of Parallel Programming (PPoPP)*, March 2007.
21. Benjamin C. Lee, David Brooks. “Illustrative design space studies with microarchitectural regression models,” *Proc. 13th IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, February 2007.
22. Benjamin C. Lee, David Brooks. “Accurate and efficient regression modeling for microarchitectural performance and power prediction,” *Proc. 12th ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, October 2006.
23. Yingmin Li, Benjamin C. Lee, David Brooks, Zhigang Hu, Kevin Skadron. “Impact of thermal constraints on multi-core architectures,” *Proc. 10th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronics Systems (ITHERM)*, May 2006.
24. Yingmin Li, Benjamin C. Lee, David Brooks, Zhigang Hu, Kevin Skadron. “CMP design space exploration subject to physical constraints,” *Proc. 12th IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, February 2006.
25. Benjamin C. Lee, Richard Vuduc, James Demmel, Katherine Yelick. “Performance models for evaluation and automatic tuning of symmetric sparse matrix-vector multiply,” *Proc. 33rd International Conference on Parallel Processing (ICPP)*, August 2004.⁶
26. Richard Vuduc, James Demmel, Katherine Yelick, Shoaib Kamil, Rajesh Nishtala, Benjamin C. Lee. “Performance optimizations and bounds for sparse matrix-vector multiply,” *Proc. IEEE International Conference for High Performance Computing, Networking, Storage and Analysis (SC)*, November 2002.⁷

⁴ Top Picks from Computer Architecture Conferences, IEEE Micro; Research Highlight, Communications ACM.

⁵ Best Paper Nomination.

⁶ Best Paper.

⁷ Best Student Paper Finalist.

Refereed Workshop Proceedings

27. Benjamin C. Lee, David Brooks. “Statistically rigorous regression modeling for the microprocessor design space,” *Proc. Workshop on Modeling, Benchmarking, and Simulation (MoBS) in conjunction with ISCA-33*, June 2006.
28. Benjamin C. Lee, David Brooks. “Effects of pipeline complexity on SMT/CMP power-performance efficiency,” *Proc. Workshop on Complexity Effective Design (WCED) in conjunction with ISCA-32*, June 2005.

Technical Reports and Manuscripts

29. Benjamin C. Lee, Mark Horowitz. “Integrated inference for hardware-software efficiency: A case study in SpMV and Smart Memories,” Technical Report No. TR-10-01, Systems Architecture Integration Laboratory, Duke University, August 2010.
30. Benjamin C. Lee. “Statistical inference for efficient microarchitectural analysis,” Ph.D. Thesis, Harvard University, May 2008.⁸
31. Yingmin Li, Kevin Skadron, Benjamin C. Lee, David Brooks. “Quantifying latency and throughput compromises in CMP designs,” Technical Report CS-2006-26, Department of Computer Science, University of Virginia, December 2006.
32. Benjamin C. Lee, Martin Schulz, Bronis de Supinski. “Regression strategies for parameter space exploration: A case study in semicoarsening multigrid and R,” Technical Report UCRL-TR-224851, Lawrence Livermore National Laboratory, September 2006.
33. Benjamin C. Lee. “An architectural assessment of SPEC CPU benchmark relevance,” Technical Report TR-02-06, Harvard University, January 2006.
34. Benjamin C. Lee, Richard Vuduc, James Demmel, Katherine Yelick, Michael de Lorimier, Lijue Zhong. “Performance optimizations and bounds for sparse symmetric matrix-multiple vector multiply,” Technical Report UCB/CSD-03-1297, University of California, Berkeley, November 2003.

Talks**Conferences and Workshops**

1. “Web search using mobile cores: Quantifying and mitigating the price of efficiency,” *37th ACM International Symposium on Computer Architecture (ISCA)*, June 2010.
2. “Phase change memory: An architecture and systems perspective,” *Workshop on Emerging Memory Technologies (EMT) in conjunction with ISCA-37*, June 2010.
3. “Architecting phase change memory as a scalable DRAM alternative,” *36th ACM International Symposium on Computer Architecture (ISCA)*, June 2009.
4. “CPR: Composable performance regression for scalable multiprocessor models,” *41st IEEE International Symposium on Microarchitecture (MICRO)*, November 2008.
5. “Efficiency trends and limits from comprehensive microarchitectural adaptivity,” *13th ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, March 2008.

⁸ Harvard University Nomination, ACM Doctoral Dissertation Award.

6. “Roughness of microarchitectural design topologies and its implications for optimization,” *14th IEEE International Symposium on High Performance Computer Architecture (HPCA)*, February 2008.
7. “Methods of inference and learning for performance modeling of parallel applications,” *12th ACM Symposium on Principles and Practice of Parallel Programming (PPoPP)*, March 2007.
8. “Statistical inference for efficient microarchitectural analysis,” *Boston Area Architecture Workshop (BARC)*, January 2007.
9. “Illustrative design space studies with microarchitectural regression models,” *13th IEEE International Symposium on High Performance Computer Architecture (HPCA)*, February 2007.
10. “Statistical inference for efficient microarchitectural and application analysis,” *IEEE/ACM International Conference for High Performance Computing, Networking, Storage and Analysis (SC)*, November 2006.⁹
11. “Accurate and efficient regression modeling for microarchitectural performance and power prediction,” *12th ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, October 2006.
12. “Statistically rigorous regression modeling for the microprocessor design space,” *Workshop on Modeling, Benchmarking, and Simulation (MoBS) in conjunction with ISCA-33*, June 2006.
13. “Effects of pipeline complexity on SMT/CMP power-performance efficiency,” *Workshop on Complexity Effective Design (WCED) in conjunction with ISCA-32*, June 2005.
14. “Performance models for evaluation and automatic tuning of symmetric sparse matrix-vector multiply,” *33rd International Conference on Parallel Processing (ICPP)*, August 2004.
15. “Optimizations and bounds for sparse symmetric matrix-vector multiply,” *SIAM Conference on Parallel Processing for Scientific Computing*, March 2004.
16. “Poster: Automatic performance tuning of sparse matrix kernels,” *SIAM Conference on Computational Science and Engineering*, February 2003.

Technical Panels

17. “Mega-servers vs. micro-blades,” *Workshop on Architectural Concerns in Large Data Centers (ACLD) in conjunction with ISCA-37*, June 2010.
18. “Emerging technologies,” *International Symposium on Nanoscale Architectures (NANOARCH) in conjunction with DAC-47*, July 2009.
19. “New memory technology,” *36th ACM International Symposium on Computer Architecture (ISCA)*, June 2009.

⁹ First Place, ACM Student Research Competition.

Invited and Other

20. "Coordinated strategies for exascale computing"
 - "—," IBM Research Triangle Park, NC, October, 2011.
 - "—," University of North Carolina, Chapel Hill, September 2011.
 - "—," Rambus, Sunnyvale, CA, August 2011.
 - "—," IBM Austin Research Laboratory, April 2011.
 - "—," North Carolina State University, March 2011.
21. "Web search using mobile cores: Quantifying and mitigating the price of efficiency,"
 - "—," University of California, Berkeley, August 2010.
 - "—," Intel Corporation, Santa Clara, CA, July 2010.
22. "Phase change memory: An architecture and systems perspective,"
 - "—," Intel Corporation, Hudson, MA, August 2010.
 - "—," Harvard University, August 2010.
 - "—," Google, Mountain View, CA, July 2010.
 - "—," Lawrence Livermore National Laboratory, May 2010.
23. "Architectural inference and the pursuit of efficiency,"
 - "—," Stanford Pervasive Parallelism Lab (PPL) Retreat, Santa Cruz, June 2010.
 - "—," University of California, Los Angeles, April 2010.
 - "—," Princeton University, March 2010.
 - "—," University of Southern California, March 2010.
 - "—," Duke University, March 2010.
 - "—," Stanford University, September 2009.
24. "Statistical inference for tractable architectural analysis,"
 - "—," University of Texas at Austin, March 2009.
 - "—," Swiss Federal Institute of Technology (ETH) Zurich, March 2009.
 - "—," University of Rochester, March 2009.
 - "—," Rutgers University, March 2009.
 - "—," Northwestern University, March 2009.
 - "—," University of Washington, Seattle, WA, March 2009.
 - "—," AMD Research, Bellevue, WA, March 2009.
 - "—," Microsoft Research, Redmond, WA, April 2008.
 - "—," IBM T.J. Watson Research Center, Yorktown Heights, NY, April 2008.
 - "—," Intel Corporation, Santa Clara, CA, June 2007.
 - "—," Intel Corporation, Folsom, CA, June 2007.
25. "Green – Energy efficient software and principled approximation," Microsoft Research Techfest, Redmond, WA with presentations to C. Mundie, R. Ozzi, R. Rashid, February 2009.
26. "CPR: Composable performance regression for scalable multiprocessor models," Intel Corporation, Santa Clara, CA, December 2007.
27. "Regression modeling strategies for parameter space exploration," Lawrence Livermore National Laboratory, Livermore, CA, September 2006.
28. "Poster: Efficient design space exploration for chip multiprocessors," Harvard University, Industrial Partnership Annual Meeting, October 2005.

Artifacts

Harvard CORE: Comprehensive Optimization via Regression Estimates (CORE) is a collection of example R scripts that construct microarchitectural performance, power regression models with correlation, association, significance analyses. (<http://www.duke.edu/~BCL15/software.html>)

Berkeley OSKI: The Optimized Sparse Kernel Interface is a collection of low-level C primitives that provide automatically tuned computational kernels on sparse matrix solves for use in solver libraries and applications (<http://bebop.cs.berkeley.edu/oski/>)

Patents

Jeremy Condit, Edmund Nightingale, Benjamin C. Lee and Engin Ipek and Christopher Frost and Doug Burger. “Hardware and operating system support for persistent memory on a memory bus,” United States Patent, USPTO Application #20100106754.

Jeremy Condit, Edmund Nightingale, Benjamin C. Lee and Engin Ipek and Christopher Frost and Doug Burger. “Hardware and operating system support for persistent memory on a memory bus,” United States Patent, USPTO Application #20100106895.

News & Press

1. John Hennessy and David Patterson. “Warehouse-scale computers to exploit request-level and data-level parallelism,” *Computer Architecture: A Quantitative Approach*, 5th edition, 2012, pp. 471–475.
2. Charles Moore. “Power efficiency as the #1 design constraint,” *Communications of the ACM (CACM), Technical Perspective*, 54(10):84, October 2011.
3. Mary Jane Irwin. “Technology scaling redirects main memories,” *Communications of the ACM (CACM), Technical Perspective*, 53(7):98, July 2010.
4. “Microsoft paper proves Atom servers can succeed,” PCMag.com. 23 April 2010.
5. James Hamilton. “Web search using small cores,” Perspectives Blog, 27 September 2009.
6. “Energy-efficiency work reaps rewards,” Microsoft Research News. 10 August 2009.
7. “Optimizing software to take advantage of PCM,” Numonyx Software Article, July 2009.

Grants

1. Principal Investigator. “CAREER: Foundations for heterogeneous datacenter design and deployment,” *National Science Foundation*, \$444K, 2012-2016.
2. Principal Investigator. “Pathfinding for emerging memory technologies,” *Google Faculty Research Award*, \$55K, 2011.
3. Principal Investigator. “Foundations for heterogeneous datacenter design and development,” *Duke University Wannamaker Foundation*, \$20K, 2011-2012.
4. Co-principal Investigator with Christos Kozyrakis (PI), Mark Horowitz, Nick McKeown, Mendel Rosenblum. “An application-driven approach to energy-efficient data centers,” *Google Focused Research Award*, \$750K, 2009-2012.
5. Fellow with Mark Horowitz (Mentor). “The Computing Innovation Fellows Project: Rethinking digital design,” *National Science Foundation*, \$280K, 2009-2010.¹⁰

¹⁰ 2010 funding declined by Fellow, who started tenure-track faculty position at Duke University.

- Research Advising**
- Doctoral Students**
Marisabel Guevara, Computer Science, Duke University, 2010 – .
Weidan Wu, Electrical and Computer Engineering, Duke University, 2010 – .
Krishna Malladi, Electrical Engineering, Stanford University (with Mark Horowitz), 2009 – .
- Undergraduate Students**
Michael Ansel, Electrical and Computer Engineering, Duke University, 2011 – .
Taejun Ham, Electrical and Computer Engineering, Duke University, 2011 – .
- Thesis Committees**
- Doctoral Students**
Azbayar Demberel (advisor Jeffrey Chase), Qing Duan (advisor Krishnendu Chakrabarty), Adam Jacobvitz (advisor Daniel Sorin), Kesari Mishra (advisor Kishor Trivedi), Mohammed Mottaghi (advisor Chris Dwyer), Brandon Noia (advisor Krishnendu Chakrabarty), Vamsidhar Thummala (advisor Shivnath Babu)
- Masters Students**
Zhiqiu Kong (advisor Landon Cox), Arpan Roy (advisor Kishor Trivedi)
- Teaching**
- Duke University, Durham NC**
Professor, Electrical and Computer Engineering, 2010 – present
– Spring 2012: Energy-efficient computer systems (ECE 299).
– Fall 2011: Advanced Computer Architecture I (ECE 252).
– Fall 2010: Energy-efficient computer systems (ECE 299).
- Stanford University, Stanford CA**
Guest Instructor, Electrical Engineering, 2009
– Autumn 2009: Advanced processor architecture (EE282a), digital systems (EE108b).
- Harvard University, Cambridge MA**
Teaching Fellow, Engineering and Applied Sciences, 2005 – 2008
– Spring 2008: Guest lecture on power modeling, digital sustainability (CS246).
– Fall 2006: Management of innovation in science, engineering (ES139/239).
– Spring 2006: Advanced architecture, power-aware systems (CS246).
– Fall 2005: Introductory computer architecture (CS146), digital logic design (CS141).
- Conference Tutorials**
Co-organizer, 2007 – 2008
– With David Brooks, Bronis de Supinski, Sally McKee, Karan Singh. “Methods of learning and inference for large design and parameter spaces,” 13th ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), March 2008.
– With David Brooks, Bronis de Supinski, Sally McKee, Karan Singh. “Inference and learning for large scale microarchitectural analysis,” 35th ACM International Symposium on Computer Architecture (ISCA), June 2007.
- Service**
- Memberships**
Institute of Electrical and Electronics Engineers (IEEE).
Association for Computing Machinery (ACM).
Society for Industrial and Applied Mathematics (SIAM).
American Association for the Advancement of Science (AAAS).

Conference Program Committees

Int'l. Green Computing Conference (IGCC) 2012.
Int'l. Symp. Perf. Analysis of Systems & Software (ISPASS) 2012.
Int'l. Parallel & Distributed Processing Symposium (IPDPS), 2012.
Int'l. Symposium on High-Performance Computer Architecture (HPCA), 2012.
Int'l. Conference on Computer Design (ICCD), 2011.
Work. on Modeling, Benchmarking, Simulation (MoBS) at ISCA, 2011.
Int'l. Conf. Supercomputing (ICS) 2011.
Int'l. Conf. Performance Engineering (ICPE) 2011.
Work. Modeling, Benchmarking, Simulation (MoBS) at ISCA 2010.
Int'l. Symp. Perf. Analysis of Systems & Software (ISPASS) 2010.
Work. Modeling, Benchmarking, Simulation (MoBS) at ISCA 2009.
Int'l Symp. Perf. Analysis of Systems & Software (ISPASS) 2009.

Conference Organizing Committees

Int'l. Symp. on Computer Architecture (ISCA) 2012.
Work. on Emerging Supercomputing Technologies (WEST) at ICS 2011.
Int'l. Symp. Perf. Analysis of Systems & Software (ISPASS) 2011.
Work. Emerging Memory Technologies (WEMT) at ISCA 2010.
Int'l Symp. Microarchitecture (MICRO) 2009.
Work. Emerging Memory Technologies (WEMT) at ISCA 2009.
Int'l Conf. Parallel Arch. & Compilation Techniques (PACT) 2009.

Conference Reviews

Int'l. Conf. Arch. Support for Programming Languages & Operating Systems (ASPLOS).
Int'l. Symp. High Performance Computer Architecture (HPCA).
Int'l. Symp. Computer Architecture (ISCA).
Int'l. Symp. Low Power Electronics and Design (ISLPED).
Int'l. Symp. Perf. Analysis of Systems & Software (ISPASS).
Int'l. Symp. on Microarchitecture (MICRO).

Journal Reviews

ACM Transactions on Architecture and Code Optimization (TACO).
ACM Transactions on Embedded Computing Systems (TECS).
ACM Transactions on Design Automation of Electronic Systems (TODAES).
IEEE Transactions on Computers (TC).
IEEE Transactions on Computer Aided Design (TCAD).
IEEE Transactions on Parallel and Distributed Systems (TPDS).
IEEE Transactions on Very Large Scale Integration Systems (TVLSI).
IEEE Computer Architecture Letters (CAL).
IEEE Micro Magazine (Micro).
Elsevier Parallel Computing (PARCO).

Grant Reviews

Department of Energy, Office of Science, Small Business Innovation Research, 2011.
Research Foundation Flanders, 2011.